WHAT IS CLAIMED IS:

1. A digital phase locked circuit for synchronizing a phase of an output clock signal with a phase of an input clock signal wherein said output clock signal is generated by dividing a master clock signal, comprising:

a phase comparing part comparing the phase of said output clock signal with the phase of said input clock signal;

a phase comparison result detecting part outputting an INC/DEC request signal for controlling a division operation based on a phase comparison signal from said phase comparing part;

an execution rate computing part computing a phase difference between said input clock signal and said output clock signal based on said INC/DEC request signal from said phase comparison result detecting part and outputting an execution rate corresponding to said phase difference; and

a clock generating part controlling a division operation for said master clock signal in accordance with said INC/DEC request signal from said phase comparison result detecting part and changing phase absorption speed of said output clock signal by masking said INC/DEC request signal in accordance with said execution rate from said execution rate computing part.

2. The digital phase locked circuit as claimed in claim 1, wherein said phase comparison

result detecting part has an up-down counter being counted up/down when a phase comparison signal being an exclusive OR signal of said input clock signal and said output clock signal from said phase comparing part is HIGH/LOW, respectively and a detecting part outputting a DEC request signal when a minimum counter value is detected and an INC request signal when a maximum counter value is detected.

3. The digital phase locked circuit as claimed in claim 1, wherein said execution rate computing part has a phase difference computing counter counting up/down a phase difference counter value thereof based on said INC/DEC request signal, respectively from said phase comparison result detecting part and setting said phase difference counter value as a computed phase difference and a phase absorption execution rate determining part outputting an execution rate corresponding to said computed phase difference with reference to a correspondence table in which correspondence between phase differences and execution rates is described.

4. The digital phase locked circuit as claimed in claim 3, wherein said execution rate computing part sets said computed phase difference by summing up a plurality of counter values for each predetermined time interval, the counter values computed by sampling said phase difference counter in a shorter time interval.

5. A digital phase locked circuit for synchronizing a phase of an output clock signal with a phase of an input clock signal wherein said output clock signal is generated by dividing a master clock signal, comprising:

a phase comparing part comparing the phase of said output clock signal with the phase of said input clock signal;

a phase comparison result detecting part referring to a comparison result from said phase comparing part and outputting a signal for increasing/decreasing a division number for dividing said master clock signal when the phase of said output clock signal proceeds forward/behind the phase of said input clock signal; and

a control part changing phase absorption speed by controlling an adoption rate of said signal for increasing/decreasing the division number for dividing said master clock signal in accordance with a phase difference between said input clock signal and said master clock signal.